TITLE OF THE INVENTION

[0005] METHOD FOR MAKING INTEGRATED OPTICAL WAVEGUIDES AND MICROMACHINED FEATURES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0010] Priority is claimed to U.S. Provisional Application Serial No. 60/206,485, filed May 23, 2000, and entitled "Single Mask Method For Making IO Waveguides And Micromachined Features", the entirety of which is incorporated herein by reference.

[0015] In addition, this is a continuation-in-part (CIP) of co-pending application Serial No. (not yet assigned: Atty. Dock. No. ACT.003) , filed May 16, 2001, and entitled "Multi-Level Optical Structure And Method Of Manufacture", which in turn is a continuation-in-part (CIP) of co-pending application Serial No. 09/853,250, filed May 9, 2001, and entitled "Multi-Level Lithography Masks." The entireties of these applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0020] The present invention generally relates to optical devices, and more particularly, the present invention relates to the fabrication of optical devices having integrated optical waveguides.

2. Description of the Related Art

[0025] Optical integrated circuit (OIC) and optical bench fabrication often involves transferring patterns to a substrate. These patterns may be used to form a variety of structures to include conductive circuit lines, planar waveguides, mesas and recesses. Typically, the desired structures are formed using lithography. Lithography may be achieved by techniques such as photolithography, x-ray lithography and e-beam lithography.

[0030] In photolithography, for example, a layer of photo-reactive film, known as photoresist, may be formed over the substrate. A photolithographic mask containing the image of a desired pattern is then placed in contact with the photoresist film. Radiation of a wavelength to which the photoresist is sensitive is incident upon the mask. The radiation passes through the transparent areas of the mask and the exposed areas of the photoresist are reactive to the radiation. The photoresist film is then chemically developed, leaving behind a pattern of photoresist substantially identical to the pattern on the mask.

[0035] The patterned photoresist on the substrate may be used in a variety of applications to form the structures referenced above. For example, a pattern photoresist may act as a mask for selective etching of a substrate. This selective etching may be used to fabricate recesses and as mesas in the substrate. In OIC and optical bench technologies, the mesas and recesses may be used for a variety of purposes, including passive alignment of optical elements.

[0040] The above described photolithographic process is often referred to as contact printing, because the mask is placed in contact with the substrate. Contact printing has facilitated the fabrication of highly integrated structures in both electrical and optical integrated circuits. However, conventional contact printing techniques have certain limitations. For example, conventional contact printing techniques generally are useful only in processing flat substrates. If a substrate has a relief (i.e. has a non-planar topography) it is exceedingly difficult to fabricate structures on the substrate by flat conventional contact printing techniques. To this end, conventional photolithographic masks are substantially flat. As a result, it is exceedingly difficult to place the mask in contact with, or in close enough proximity to, all points on the surface of a substrate to enable accurate image projection onto the substrate. In regions of the substrate where the photolithographic mask is not in contact with, or in close enough proximity to, the substrate, diffractive effects result in poor resolution and ultimately a poor transfer of the pattern from the mask to the photoresist.

[0045] The above referenced limitations of image lithography processing typically result in inaccurate location and spacing of features in a multi-level substrate. These inaccuracies are unacceptable as the integration of various elements at multiple levels in OIC's and optical bench technologies gains industry acceptance. Accordingly, what is needed are optical integrated circuits and optical benches which incorporate a variety of features at multiple levels which overcome the inaccuracies of conventional structures and methods of manufacture as referenced above.

SUMMARY OF THE INVENTION

[0050] According to an aspect of the present invention, an optical device is fabricated having at least one integrated waveguide and at least one micro-machined feature. Although not so limited, exemplary micro-machined features include grooves, recesses and inclined surfaces formed in the substrate surface. A mask layer is deposited over a surface of a substrate structure, and the mask layer is patterned to obtain a mask pattern over the surface of the substrate structure. A first etching process is then carried out for obtaining the at least one integrated optical waveguide core at the surface of the substrate structure, and a second etching process is carried out for obtaining the at least one micro-machined feature at the surface of the substrate structure. Advantageously, the same previously formed mask pattern is used as a mask in both the first and second etching processes, thereby resulting in accurate positioning of the waveguide core relative to the micro-machined feature.

BRIEF DESCRIPTION OF THE DRAWINGS

[0055] The invention is best understood from the following detailed description when read with the accompanying drawings. It is emphasized that the various features are not necessarily drawn to scale. In fact, the dimensions may be arbitrarily increased or decreased for clarity of discussion.

[0060] FIGs. 1(a) through 1(m) are side views for describing a method of fabricating an optical device according to an embodiment of the present invention.

[0065] FIGs. 2(a) through 2(i) are top views for describing a method of fabricating an optical device according to another embodiment of the present invention.

[0070] FIGs. 3(a) through 3(m) are side views for describing a method of fabricating an optical device according to the embodiment of FIGs. 2(a) through 2(i).

[0075] FIG. 4 is a top view for describing a variation of the embodiment of FIGs. 2(a) through 2(i).

[0080] FIGs. 5(a) and 5(b) are side views corresponding to the variation of FIG. 4.

[0085] FIG. 6 is a side view of another embodiment of the present invention.

[0090] FIGs. 7(a) through 7(e) are side views for describing a method of fabricating an optical device according to another embodiment of the present invention.

[0095] FIGs. 8(a) through 8(l) are side views for describing a method of fabricating an optical device according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0100] In the following detailed description, for purposes of explanation and not limitation, exemplary embodiments disclosing specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one having ordinary skill in the art having the benefit of the present disclosure, that the present invention may be practiced in other embodiments that depart from the specific details disclosed herein. Moreover, descriptions of well-known devices, methods and materials may be omitted so as to not obscure the description of the present invention.

[0105] As will become apparent below, the present invention is at least partially characterized by the use of the same, preferably planar, mask pattern as an etching mask in defining the horizontal location of micro-machined (etched) features at the substrate surface of an optical device relative to the waveguide cores also at the substrate surface of the optical device. Although not so limited, exemplary micro-machined features include grooves, recesses and inclined surfaces formed in the substrate surface for any of a variety of purposes. For example, grooves may be machined (etched) into the substrate surface for holding optical fibers which are to be optically coupled to the integrated waveguide cores. Also, recesses may be formed for holding spherical elements which function as guide balls in an optical switch device. Likewise, inclined substrate surfaces may fabricated as alignment surfaces for accurate mounting of the optical device into a system. The accurate horizontal positioning of these features relative to the integrated waveguide cores fosters accurate optical coupling between the integrated waveguide cores and external and/or internal components.

[0110] An illustrative embodiment of a method of fabricating an optical device according to the present invention will now be described with reference to FIGs. 1(a) through 1(m) of the drawings. Throughout these figures, like elements are designated by the same reference numbers.

[0115] FIG. 1(a) generally depicts a substrate 101. In this embodiment, the substrate 101 is a silicon substrate. However, any of a variety of substrate structures may be adopted, including silicon-on-insulator (SOI) substrates.

[0120] Using known masking and etching techniques, a pit 102 is etched in the substrate 101 as shown in FIG. 1(b). The pit 102 is optionally formed so as to define inclined sidewalls 103. Then, as shown in FIG. 1(c), a cladding material layer 104 is deposited over the surface of the substrate 101 and within the pit 102. In this embodiment, the cladding material layer 104 is formed of silicon dioxide (SiO_2), although other materials may be readily adopted.

[0125] The structure of FIG. 1(c) is then planarized to obtain the structure shown in FIG. 1(d). Here, the cladding layer material 104 is contained with the pit 102, and the remaining surface of the substrate 101 is exposed.

[0130] Turning to FIG. 1(e), a core material layer 105 is deposited over the surface of the structure of FIG. 1(d) so as to cover the exposed surface of the substrate 101 and the surface of the cladding material layer 104 contained within the pit 102. In this embodiment, the core material layer 105 is formed of silica. However, other materials may be used, such as silicon and silicon nitride.

[0135] A mask layer 106a/106b is then deposited and patterned over the core material layer 105. In particular, as shown in FIG. 1(f), the patterned mask layer includes portions 106a which define etched features and portions 106b which define waveguides. The patterned mask layer may be formed of a metal such as chromium (Cr). Other materials

may be used, however, such as aluminum, titanium, copper, gold, nickel, metal silicides, silicon nitride, and other etch resistant materials.

[0140] Exposed portions of the core material layer 105 are then removed by reactive ion etching (RIE) as illustrated in FIG. 1(g). As a result, the remaining core material layer is defined by etched feature portions 105a and waveguide portions 105b. The mask layer portions 106b (FIG. 1(f)) are then removed from the respective tops of the waveguide portions 105b, and another cladding material layer 107 is deposited over a resultant structure as shown in FIG. 1(h). Again, the cladding material layer 107 may, for example, be formed of SiO_2 or other materials.

[0145] Turning to FIG. 1(i), a mask 108 is deposited over the cladding material layer 107 so as to cover the waveguide portions 105b and partially overlap the mask layer portions 106a and underlying etched feature portions 105a. Another etch process (e.g., wet etching or RIE) is then performed down to the silicon substrate to obtain the structure illustrated in FIG. 1(i). As shown, the mask layer portions 106a and underlying etched feature portions 105a remain on the surface of the silicon substrate 101.

[0150] The structure of FIG. 1(i) is then subjected to a wet etch to obtain the structure of FIG. 1(j) in which inclined surface features 109 are formed at opposite sides of the silicon substrate 101. Note that the inclined surface features 109 are defined here by the same mask pattern what was previously used to defined the waveguide portions 105a of the core material layer. Also note that the inclined surface features 109 may actually define half of a V-shaped groove in the case where another device is being

simultaneously formed in the substrate 101 adjacent to the device illustrated in the drawings.

[0155] Another mask is applied as shown in FIG. 1(k). In particular, the mask includes a portion 110a which covers the waveguide portions 105b of the core layer, and portions 110b which cover the inclined surfaces 109 of the substrate 101. This structure is then etched in hydroflouric acid (HF) to obtain the structure shown in FIG. 1(l). As shown, the side surfaces 111a of the upper cladding layer 107 may exhibit a slight concave configuration. The mask portions 110a and 110b are then removed to obtain the device structure of FIG. 1(m) having the waveguide cores 105b sandwiched between lower and upper cladding layers 104 and 107, respectively.

[0160] In the process described above, the distance D of FIG. 1(m) is a horizontal distance between the waveguide core 105a and the inclined surface feature 109. Since the same mask pattern 106a/106b is used to etch both the waveguide 105a and the feature 109, this distance D may be precisely set, and the device characteristics and alignment tolerances are thereby improved.

[0165] Another illustrative embodiment of the present invention will now be described with reference to the top views of FIGs. 2(a) through 2(i) and the side views of FIG. 3(a) through 3(n). Throughout these figures, like elements are designated by the same reference numbers. In this embodiment, a generally V-shaped groove (micro-machined feature) is aligned with an integrate optical waveguide core(s).

[0170] FIGs. 2(a) and 3(a) illustrate a structure which is similar to that obtained in FIG. 1(e) described above. That is, in FIGs. 2(a) and 3(a), reference number 201 denotes a

substrate, reference number 204 denotes a lower cladding material layer, and reference number 205 denotes a core material layer. A mask layer is deposited over the cladding material layer 205 as shown in FIGs. 2(b) and 3(b). The mask layer includes a first portion 206a which surrounds and thereby defines a groove region 213, and a second portion 206b which covers and thereby defines a waveguide region 214. As shown, the waveguide region 214 and the groove region 213 are aligned with one another along their respective lengths. Also, for simplicity the drawings depict a continuous second mask portion 206b. However, the mask portion 206b can actually comprise a number of parallel masks for defined a corresponding number of parallel waveguide cores within the waveguide region 214.

[0175] Turning to FIGs. 2(c) and 3(c), the exposed portions of the core material layer 205 are removed by RIE using the first and second mask portions 206a and 206b as a mask. As a result, a portion 205a of the core material layer remains below the first mask portion 206a, and another portion 205b of the core material layer remains below the second mask 206b. Then, referring to FIGs. 2(d) and 3(d), the portion 206b of the mask layer is removed from atop the portion 205b of the core material layer within the waveguide region 214.

[0180] An upper cladding material layer is then deposited over the entire surface of the structure shown in FIGs. 2(d) and 3(d). The resultant configuration is depicted in FIGs. 2(e) and 3(e) in which reference number 207 denotes the upper cladding material layer. Then, as shown in FIGs. 2(f), 3(f) and 3(g), a mask 208 is deposited over the upper cladding material layer 207 such that edges 231 of an opening 230 thereof are aligned

with the portion 206a. Here, FIG. 3(f) is a side view of FIG. 2(f), and FIG. 3(g) is a cross-sectional view of FIG. 2(f) along line 2-2'.

[0185] Exposed portions of the upper cladding material layer 207 are then removed by RIE using the mask 208 as a mask, whereby the surface of the substrate 201 within the groove region 213 becomes exposed. The resultant configuration is shown in FIGs. 2(g), 3(h) and 3(i). FIG. 3(h) is a side view of FIG. 2(g), and FIG. 3(i) is a cross-sectional view of FIG. 2(g) along line 4-4'.

[0190] The configuration of FIGs. 2(g), 3(h) and 3(i) is then subjected to a wet etching process using the mask 208 as a mask, to thereby form a groove 240 in the exposed surface portion of the substrate 201. Note that the groove 240 is defined here by the same mask pattern what was previously used to defined the waveguide portions 205a of the core material layer. The mask 208 is then removed, and the resultant configuration is illustrated in FIGs. 2(h), 3(j) and 3(k), where FIG. 3(j) is a side view of FIG. 2(h), and FIG. 3(k) is a cross-sectional view of FIG. 2(h) along line 6-6'. As shown in these figures, the groove 240 extends lengthwise in alignment with the waveguide region 214.

[0195] The groove 240 and the waveguide region 214 are then precisely spaced apart by cutting transversely therebetween into the substrate 201 with a dicing blade. The resultant configuration is shown in FIGs. 2(i), 3(l) and 3(m), where FIG. 3(l) is a side view of FIG. 2(i), and FIG. 3(m) is a cross-sectional view of FIG. 2(i) along line 8-8'. Here, reference number 260 denotes the dicing saw cut. In this device, the waveguide region 214 and the groove 240 (i.e., "feature") are precisely aligned since the same mask pattern was used in the fabrication of each.

[0200] A modification of the previous embodiment is shown in FIGs. 4, 5(a) and 5(b), where FIG. 5(a) is a cross-sectional view of FIG. 4 along line 10-10' after the RIE process, and FIG. 5(b) is a cross-sectional view of FIG. 4 along line 10-10' after the wet etch process. Here, the first mask portion 406a extends in two parallel strips on either side of the groove region 413. This is contrasted with the configuration of the previous embodiment in which the first mask portion surrounds the groove region on three sides. Otherwise, the process is carried out in the same manner as the previous embodiment.

[0205] FIG. 6 illustrates an alternative process in which a layer of silicon nitride 680 is disposed under the core material layer in a vicinity of the machined features. Silicon nitride exhibits superior masking properties (compared to SiO_2) for anisotropic wet etching of the silicon substrate 601.

[0210] Another embodiment of the present invention will now be described with reference to FIGs. 7(a) through (e). In this embodiment, the core material layer is not etched to define the micro-machined features until after the waveguides are defined.

[0215] FIG. 7(a) illustrates a structure similar to that described above in connection with FIG. 1(f). In particular, a lower cladding layer 704 is contained with a pit 702 formed in the surface of a substrate 701. A core material layer 705 extends over the surface of the substrate 701 and the lower cladding layer 704, and a mask pattern is formed over the core material layer 705. The mask pattern includes etched feature portions 706a and waveguide portions 706b.

[0220] Turning to FIG. 7(b), a mask 790 is formed over the core material layer 705 and the mask pattern 706a/706b so as to have an opening aligned with the lower cladding

layer 704. The exposed portions of the core material layer 705 are then removed by RIE and the mask 790 is removed to obtain the structure depicted in FIG. 7(c). Here, reference number 705b denotes the waveguide portions of the core material layer remaining after etching.

[0225] The portions 706b of the first mask are then removed, and an upper cladding layer 707 is deposited as shown in FIG. 7(d). This structure is then subjected to an etch process (e.g., wet etching or RIE) to remove portions of the upper cladding layer 707 and thereby define the machined features as shown in FIG. 7(e). The process then proceeds as in the first described embodiment (see FIG. 1(i)). One advantage of the present embodiment is that the machined features can be more accurate since the core layer defining the machined features is etched only once.

[0230] Yet another illustrative embodiment of the present invention will now be described with reference to FIGs. 8(a) through 8(l) of the drawings.

[0235] Using known masking and etching techniques, a pit 802 is etched in a substrate 801 as shown in FIG. 8(a). In this embodiment, the substrate 801 is a silicon substrate. As before, however, any of a variety of substrate structures may be adopted, including silicon-on-insulator (SOI) substrates. The pit 802 is optionally formed so as to define inclined sidewalls 803.

[0240] Then, as shown in FIG. 8(b), a cladding material layer 804 is deposited over the surface of the substrate 801 and within the pit 802. In this embodiment, the cladding material layer 804 is formed of silicon dioxide (SiO_2), although other materials may be adopted. Deposition of the cladding material layer 804 is halted prior to completely

filling the pit 802, such that an upper surface of cladding material layer 804 is a displaced a distance "D" below a level of an upper surface of the substrate 801.

[0245] Turning to FIG. 8(c), a core material layer 805 is deposited over the surface of the cladding material layer 804. In this embodiment, the core material layer 105 is formed of silica. However, other materials may be used, including but not limited to silicon and silicon nitride. The structure of FIG. 8(c) is then planarized to obtain the structure of FIG. 8(d). As shown, both the core material layer 805 and the cladding layer material 804 are contained with the pit 802, and the remaining surface of the substrate 801 is exposed.

[0250] A mask layer is then deposited and patterned over the surface of the structure shown in FIG. 8(d). In particular, as shown in FIG. 8(e), the patterned mask layer includes portions 806a which define etched features and portions 806b which define waveguides. The patterned mask layer 806a/806b may be formed of a metal such as chromium (Cr). Other materials may be used, however, such as aluminum, titanium, copper, gold, nickel, metal silicides, silicon nitride, and other etch resistant materials.

[0255] A mask 820 is then deposited with an opening that exposes the pit 802, and portions of the core material layer 805 are then removed by RIE as illustrated in FIG. 8(f). As a result, the remaining core material layer is defined by the waveguide portions 805b. The mask layer portions 806b are then removed from the respective tops of the waveguide portions 805b, and another cladding material layer 807 is deposited over a resultant structure as shown in FIG. 8(g). Again, the cladding material layer 807 may, for example, be formed of SiO_2.

[0260] Turning to FIG. 8(h), a mask 808 is deposited over the cladding material layer 807 so as to cover the waveguide portions 805b and partially overlap the mask layer portions 806a and underlying etched feature portions 805a. Another etch process (e.g., wet etching or RIE) is then performed down to the silicon substrate 801 to obtain the structure illustrated in FIG. 8(i). As shown, the mask layer portions 806a remain on the surface of the silicon substrate 801.

[0265] The structure of FIG. 8(i) is then subjected to a wet etch to obtain the structure of FIG. 8(j) in which inclined surface portions 809 are formed at opposite sides of the silicon substrate 801. It is noted that the inclined surface portions 809 may actually define half of a V-shaped groove in the case where another device is being simultaneously formed in the substrate 801 adjacent to the device illustrated in the drawings.

[0270] Another mask is applied as shown in FIG. 8(k). In particular, the mask includes a portion 810a which covers the waveguide portions 805b of the core layer, and portions 810b which cover the inclined surface features 809 of the substrate 801. This structure is then etched in HF to obtain the structure shown in FIG. 8(k). As shown, the side surfaces 811a of the upper cladding layer 807 may exhibit a slight concave configuration. The mask portions 810a and 810b are then removed to obtain the device structure of FIG. 8(l) having the waveguides 805b sandwiched between lower and upper cladding layers 804 and 807, respectively.

[0275] As with the previously embodiments, the horizontal distance between the waveguide cores 805a and the inclined surface feature 809 is precisely set since the same

mask pattern 106a/106b is used to etch both the waveguide 805a and the feature 809, and the device characteristics and alignment tolerances are thereby improved.

[0280] While the invention has been described in detail with respect to a number of exemplary embodiments, it is clear that various modifications of the invention will become apparent to those having ordinary skill in art having had benefit of the present disclosure. Such modifications and variations are included in the scope of the appended claims.